UNIFYING METHODOLOGIES FOR HIGH FAULT COVERAGE CONCURRENT AND OFF-LINE TEST OF DIGITAL FILTERS*

Ismet Bayraktaroglu

Computer Science & Engineering Department
University of California, San Diego
La Jolla, CA 92093
ibayrakt@cs.ucsd.edu

Alex Orailoglu

Computer Science & Engineering Department
University of California, San Diego
La Jolla, CA 92093
alex@cs.ucsd.edu

ABSTRACT

A low-cost on-line test scheme for digital filters that additionally provides an off-line BIST solution is proposed. The scheme utilizes an invariant of the digital filter in order to detect on-line possible circuit malfunctions. The on-line checking hardware is shared with off-line BIST. The analysis performed indicates that exact 100% fault secureness is attained when the digital filter is designed according to design criteria that we identify in the paper. Furthermore, fault simulations show near 100% fault coverage for off-line BIST.

1. INTRODUCTION

Both the numbers and application arenas of DSPs have shown tremendous growth in the last two decades. The growth has been largely fuelled by enhancements in VLSI technology which have spurred the implementation of sophisticated functionality on high-speed hardware. In turn, increased complexity and high clock frequency together with consumer-driven reliability constraints have raised the importance of both off-line and on-line test. At the same time though, increased complexity together with higher clock frequencies have pushed test costs up, since test development as well as ATE costs have increased tremendously. Therefore, low-cost BIST and on-line test solutions have been frequently sought.

In this study, we propose a low-cost on-line test solution for digital filters capable of supporting off-line BIST and reducing the cost of on-line test hardware by trading off latency to fault detection. The method proposed in this study utilizes a functional invariant of a digital filter, and is therefore comparable to algorithm-based fault detection [8]. In contrast to algorithm-based techniques which utilize certain relationships between the input and output space at a given time instance, the proposed scheme utilizes an input/output relation, which holds only if a wide time range is considered. Use of such a technique introduces latency to the fault detection process. Such latency is inversely proportional to the magnitude of fault effects, thus ensuring rapid fault security for faults with large magnitudes. Furthermore, the scheme we propose has appreciably lower area overhead than comparable methods. Such area reduction benefits are accentuated as the hardware utilized for the proposed on-line test is similar to that of arithmetic pattern generators [11] and can thus provide the basis of a combined low-cost on-line/off-line test scheme.

In the experiments performed in this study, a high-pass and a low-pass filter are implemented and 100% fault coverage is attained for both filters within a reasonable latency. Design constraints, such as monotonicity of fault effects, necessary for complete fault coverage, introduce extra area overhead; no performance overhead, unlike scan, exists in the scheme we propose though. A high coverage off-line BIST solution can be incorporated at the small additional cost of 1% area overhead.

We review in section 2 previously developed off-line and on-line test schemes for DSP and motivate the rationale and the application areas for the proposed scheme. While section 3 outlines the determination of the proposed invariant, section 4 further extends the discussion to include how the invariant is utilized in this study. Section 5 provides results and associated explanatory remarks. We finish with concluding remarks in section 6.

2. PREVIOUS WORK & MOTIVATION

Off-line test schemes developed for digital filters outweigh comparable schemes developed for on-line test. In [2], a short sequence of functional test patterns is proposed, providing fault coverages in excess of 90%; high functional coverage is proven through analysis and high structural coverage is substantiated through fault simulations. Goodby and Orailoglu in [3] develop built-in self-test techniques capable of 100% fault coverage through RT and gate level op-

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timizations that eliminate redundant and random-pattern resistant faults. In [7], a low-cost, parameterizable BIST solution for digital filters is developed through utilization of arithmetic pattern generators.

On-line test approaches can be grouped in three categories: BIST, test vector, and invariant-based approaches. A BIST-based approach [6] utilizes the idle clock cycles of the functional units in order to implement on-line checking. Test vector based approaches, such as the input vector monitoring technique introduced in [12], require observation of a predetermined set of test vectors during normal operation of the circuit. Another set of schemes utilizes an invariant property of the function implemented by the circuit. The invariant could be the function itself in the case of duplication [5], or a linear approximation of a non-linear function as in [1]. In the case of high performance designs that are implemented by residue number systems, a redundant residue [10] can be utilized to provide an invariant. In [8], *Parseval's theorem* [9] is utilized for the FFT algorithm so as to achieve concurrent detection of faults.

The number of techniques previously developed for on-line test of digital filters is limited; furthermore, the ones proposed either require high area overhead or are solely applicable to high performance filters that utilize a residue number system. The current invariant-based approaches, on the other hand, are applicable only when a time-independent relation exists between input and output. None of these techniques, furthermore, is capable of supporting an integrated low-cost off-line built-in test solution. To surpass such limitations, we introduce in this study a low-cost technique capable of providing an integrated off-line test solution and applicable even when no time-independent invariant relation exists.

3. INVARIANT DETERMINATION

In this section, we introduce the invariant utilized in this work and outline its derivation. The functionality of an FIR filter is defined by the following equation.

$$y[n] = \sum_{k=0}^{M} h_k x[n-k] \tag{1}$$

In this equation, the h_k's constitute the coefficients that govern the frequency characteristics of the filter. We utilize as an invariant the frequency response of the filter at $w = 0$, which corresponds to the DC gain of the filter. In order to be able to utilize the invariant ($\mathcal{I}$) in an on-line test scheme, we start by taking the infinite summation of both sides of equation 1. Minor algebraic manipulations yield equation 2, an alternative way of expressing the DC gain of a filter.

$$\mathcal{I} = \sum_{k=0}^{M} h[k] \quad = \quad \frac{\sum_{n=-\infty}^{+\infty} y[n]}{\sum_{n=-\infty}^{+\infty} x[n]} \tag{2}$$

However, for a relation to be applicable in an on-line test environment, it should be determinable from a finite set of input/output values. The same relation over a limited time range yields:

$$\sum_{n=0}^{N} y[n] \quad = \quad \mathcal{I} \sum_{n=0}^{N} x[n] + \mathcal{T} \tag{3}$$

wherein it can be shown that the tolerance, $\mathcal{T}$, is bound by the following:

$$|\mathcal{T}| \leq \mathcal{T}_{max} = 2x_{max} \sum_{n=1}^{M} \left| \sum_{k=n}^{M} h_k \right| \tag{4}$$

In equation 4, x_{max} denotes the maximum input signal magnitude. $\mathcal{T}_{max}$ depends only on filter coefficients and the maximum input magnitude. As can be seen in equation 3, an increase in the number of inputs results in a diminution of the effective impact of $\mathcal{T}$ on invariance. In the next section, we propose an implementation of an on-line test scheme for digital filters with low cost and reasonable fault detection latency.

4. DESIGN ISSUES

In this work, the relation derived in the previous section is utilized for on-line fault detection as in the following form:

$$\left| \mathcal{I} \sum_{n=0}^{N} x_n - \sum_{n=0}^{N} y_n \right| \leq \mathcal{T}_{max} \tag{5}$$

As shown in figure 1, an adder and a register is introduced both to the input and output of the circuit in order to evaluate $\sum_{n=0}^{N} x_n$ and $\sum_{n=0}^{N} y_n$. The shaded multiplexers in the figure are utilized only if an off-line BIST solution is required. The accumulated input is multiplied with $\mathcal{I}$ and the accumulated output is subtracted. The absolute value of the difference is compared subsequently with $\mathcal{T}_{max}$, computed off-line. If the result is not within the acceptable tolerance range, an error is reported.

The fault detection capability of a scheme based on equation 5 stems from the assumption of fault effect accumulation. The latency of fault detection depends on the value of $\mathcal{T}_{max}$. We analyze both fault detection and latency issues in this work. Accumulation of fault effects necessitates monotonicity of the fault effects on the output. As long as

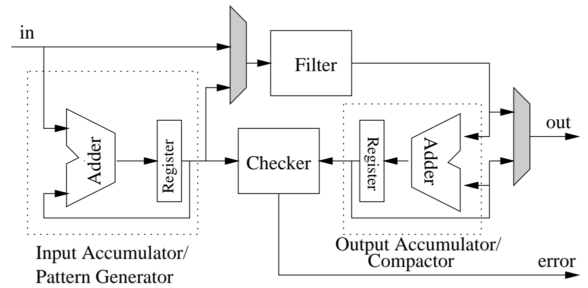

Figure 1: On-line/off-line BIST hardware

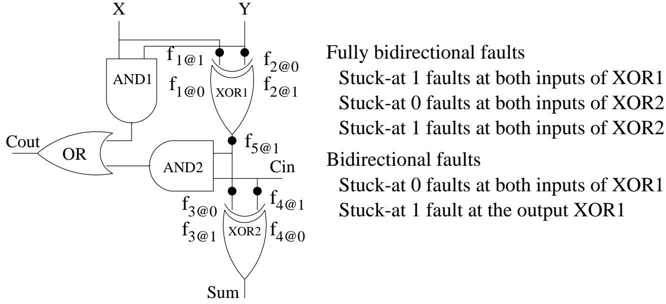

Figure 2: A typical full-adder implementation

the faults produce monotonic errors at the outputs, the errors will be accumulated to exceed eventually the value of $\mathcal{T}_{max}$. At the RT level, with no resource sharing, the linearity of the filter structure guarantees that monotonic fault effects at the block level result in monotonic output effects.

For an analysis at lower levels of design, a gate level implementation needs to be identified. We outline the type of analysis and associated issues by focusing on ripple-carry adders. As the adder's functionality at the input/output level as well as in the full-adder decomposition level is linear, the monotonicity of the input and output faults of full-adders is guaranteed by functionality. However, the monotonicity of the faults internal to the full-adders depends on the gate level implementation.

A simple full-adder implementation, as illustrated in Figure 2, is utilized for analysis of faults internal to full-adder cells. Simulation is performed in order to record the outputs of this full adder circuit for all possible faults. The simulation results indicate that 9 out of the 26 simulated faults violate the monotonic fault effect requirement. Simulation results indicating the direction of the error for those 9 faults are reported in table 1. A NAND/NAND implementation for the same functionality reduces the number of bidirectional faults to three. Even though various other modifications that further reduce the number of bidirectional faults can be entertained, any 2-level implementation of full-adders can be shown to provide complete monotonicity by analyzing the effects of the faults at the inputs and outputs of both the AND and OR levels. We utilize a 2-level implementation of full-adders in the rest of this paper.

We continue the analysis with a discussion of fault de-

Inputs	$f_{1@0}$	$f_{2@0}$	$f_{5@1}$	$f_{1@1}$	$f_{2@1}$	$f_{3@0}$	$f_{4@0}$	$f_{3@1}$	$f_{4@1}$
000	=	=	↑	↑	↑	=	=	↑	↑
001	=	=	↑	↑	↑	=	↓	↓	=
010	=	↓	=	↓	=	↓	=	=	↓
011	=	↓	=	↓	=	↑	↑	=	=
100	↓	=	=	=	↓	↓	=	=	↓
101	↓	=	=	=	↓	↑	↑	=	=
110	↑	↑	↑	=	=	=	=	↑	↑
111	↓	↓	↓	=	=	=	↓	↓	=

Table 1: Effects of non-monotonic faults on the full-adder's outputs

tection latency. The effect of a fault at the nth bit position of an adder to the output will be $2^{-(B-n)}$, where B is the output width of the filter. Therefore, in order for a fault at the nth bit position to be detected, it has to be activated $2^{B-n}\mathcal{T}_{max}$ times; the faults at the sign-bit position will be detected after $\mathcal{T}_{max}$ activations and the faults at the least significant bit will require 2^{B-1} times as many activations. This wide divergence in the number of patterns required is correlated with the magnitude of the fault effect. In addition to the positive correlation with fault effect magnitude, the likelihood of fault activation also impacts detection latency. If a fault is unlikely to be activated, it will not be rapidly detected.

Ascertaining fault security levels for an on-line application necessitates knowledge of the input patterns. While a knowledge of the distribution of the input patterns may be usable to provide an analytical understanding of the fault security levels attained, such analysis provides results that are limited and applicable only for narrow domains. Assuming no prior knowledge of the input patterns in an on-line environment necessitates a reliance on fault simulation methods for ascertaining fault security levels. We utilize simulation-based techniques with random patterns in order to establish fault security levels of our scheme, as shown in the next section.

5. RESULTS

Two 13-tap filters, one high-pass (14-bit output) and one low-pass (12-bit output), are implemented and fault simulations for the on-line test scheme are performed on both filters. The simulations for off-line test, on the other hand, are only performed for the low pass filter. The hardware added for on-line test is also utilized for off-line test with the addition of two multiplexers that are shown as shaded in figure 1.

While performing off-line test, a test signal causes the filter inputs to be supplied from the arithmetic pattern generator. The initial seed and increment for the pattern generator are supplied from the circuit inputs. The outputs are compacted at the output accumulator and observed at the output at the end of the off-line test session through the output multiplexer. The fault simulation results for off-line test are presented in figure 3 for four types of arithmetic pattern generators [11]. The first 1000 patterns are standard ABIST patterns. As can be seen in figure 3, the fault coverage curves level off after 600 patterns. This is due to the fact that ABIST is not capable of activating the faults at the sign bit of most adders. These faults usually require high variance input patterns [4]. Therefore, a set of high variance patterns generated by the same off-line hardware with an increment of 1111110111 is applied in order to detect the remaining sign bit faults. The fault coverage levels, except for the 5-bit subspace optimal case, thus exceed 99.9%.

Figure 4 shows the results of fault simulations performed

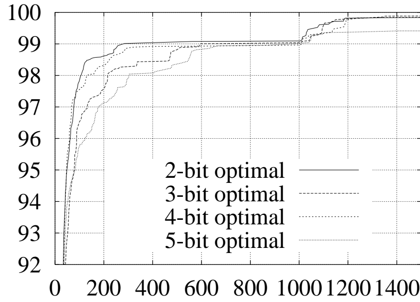

Figure 3: Fault coverages for off-line test

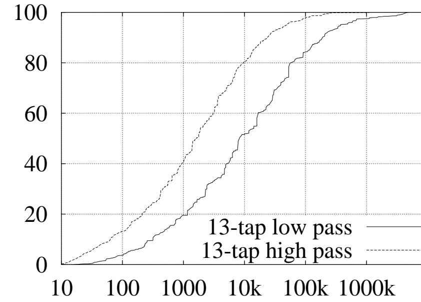

Figure 4: Fault secureness for on-line test

for on-line test on both filters. In both cases, 100% fault security is attained. The fault security levels are higher then the off-line test results since fault security measures the ratio of the faults activated to the ratio of faults detected, whereas fault coverage measures the ratio of the number of faults detected to the number of irredundant faults.

In order to further differentiate among high versus low bit faults, analysis of the bit positions of the faults caught at analogous pattern counts needs to be undertaken. We report on this analysis in table 2, which confirms the magnitude-based differential latency aspect, outlined in section 4.

The impact of the scheme on performance is negligible since the scheme solely observes the inputs and outputs of the circuit. The area overhead, though, is significant for smaller designs. For example, the area overhead for the experimental benchmarks hovers around 25%. Nonetheless, for filter designs that are larger and more typical of industrial use, the overhead for the proposed scheme constitutes a much smaller proportion as it is invariant to the size of the circuit. As an example, the area overhead for a 60-tap filter can be estimated to be only 5%, comparable to the overhead of scan-based techniques, which constitute the typical solution space in current designs. Such scan-based solutions neither have concurrent test capabilities nor can they provide at-speed test. They furthermore impact the performance of the filter by introducing multiplexers between the combinational logic and the flip-flops. Not only does the proposed scheme provide both on-line and off-line test solutions but it does so with an overhead essentially comparable to traditional scan-based solutions.

6. CONCLUSION

A time-extended invariant for concurrent test of digital filters, capable furthermore of providing high fault coverage for off-line BIST, is proposed. The fault detection capability of the on-line scheme is analyzed and the design constraint of monotonicity is identified as instrumental for ensuring 100% fault secureness. Two filters are designed and fault simulations are performed for both on-line and off-line test. 100% fault secureness with no false alarms in the case of on-line test as well as fault coverage in excess of 99.9% in the case of off-line BIST test are thus achieved.

	Bit positions in the adder													
Patterns	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256	87	68	75	52	7	0	0	0	0	0	0	0	0	0
512	93	76	83	79	50	5	0	0	0	0	0	0	0	0
1024	93	80	88	82	76	38	2	0	0	0	0	0	0	0
2048	93	87	93	91	88	66	38	2	0	0	0	0	0	0
4096	100	95	98	96	96	82	67	34	1	0	0	0	0	0
8192	100	97	100	100	100	90	84	75	60	31	6	0	0	0

Table 2: Percentage fault coverage for bit-positions

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