Ismet Bayraktaroglu

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Interests: Design and Verification, Test Pattern Compression, Logic and Memory BIST Techniques, Fault Diagnosis and Tolerance

Education:
Ph.D. in Computer Science & Engineering, UC San Diego, 1996-2001.
Thesis: *Extending the Reach of Self-Test Approaches in VLSI*
M.S. in Electrical and Electronic Engineering, Bogazici University, Turkey, 1994-1996.
Thesis: *Circuit Level Simulation Based Training Algorithms for Analog Neural Networks*
B.S. in Electrical and Electronic Engineering, Bogazici University, Turkey, 1989-1994.
B.S. Senior Project: *Design and Implementation of a PLC with MC6803*
B.S. in Physics, Bogazici University, Turkey, 1989-1994.

Awards:
Sun Microsystems, Kickbutt Team Award, 2007
Sun Microsystems Attaperson Award, 2002
IBM Fellowship Award, 2000/2001.
UCSD Flaviu Cristian Research Award, 1999.
Intel SRA Recognition Award, 1997.
Graduated ranked first from Bogazici University in 1994.
Vehbi Koc Foundation award for academic excellence, 1989.
Placed 5th in 1989 Turkish University Entrance Exam among 1 million participants.

Patents
Method and apparatus for generating test pattern for integrated circuit design; 6925617
Concurrently programmable dynamic BIST; 7062694
Instruction Based Built in self test of external memory; 7020820
Method and apparatus for generating and verifying libraries for ATPG tool; 7065724
Instruction Based Built in self test of memory interconnect; 7096393

Expertise:
Programming in C, C++, Assembly, Java, ML, Verilog, SystemC, Vera, Perl, TCL/TK
Computer Platforms: Unix, Windows.

Employment:
Staff Engineer, Sun Microelectronics, 2001 – present.
- Development of a Vera based verification environment for DFT features
- Verification of all DFT features for a Sun Sparc Processor
- Implementation of a programmable Memory BIST IP generator with verification environment
- Development of ATPG based functional test methodology
- Development of a speed path analysis tool to automatically generate monitors to measure speed path coverage of functional tests
- Development of a methodology to run functional tests from internal cache structures to avoid high speed IOs
- Analysis and Optimization of VCS simulation performance
- Formal verification of a load/store arbitration unit
- OpenSPARC T1 RTL optimizations for FPGA port and netlist verification
- OpenSPARC T2 SystemC implementation of 10GE Ethernet interface and its verification

Instructor, University of California, San Diego Summer 2000
Taught "Components & Design Techniques for Digital Systems" class

Intern, STMicroelectronics, July-September 1998
Work on implementation BIST for Microprocessor Caches
Research Assistant, University of California, San Diego, 1998 - 2001
Performed research in concurrent testing, built-in self-test, diagnosis, and test pattern compression. Learned verilog, C/C++, Java. Used Synopsys design compiler and Mentor graphics FastScan tools. Published over 20 papers.
Intern, Intel PCD, July-September 1997
Work on PRPG-based BIST Techniques.
Teaching Assistant, University of California, San Diego, 1996-1998
Taught in "Programming Languages", "Computer-Aided Design of VLSI Circuits", "Logic Design" and "Computer Architecture"
Teaching Assistant, Bogazici University, Turkey, 1994-1996
Taught in "Fundamentals of Electrical Engineering", "Electrical Network Laboratory", "Signals and Systems" and "Control Systems Laboratory"
Research Assistant, Bogazici University, Turkey, 1994 – 1996.
Worked in the project *Design and Implementation of a High Speed Direct Drive Robotic Manipulator*
Software Engineer, YENICAG, Turkey, Satellite TV Receiver Development Group, 1995-1996.
Worked on assembly based software development.
Intern, STFA, Turkey, Technical Consulting Services Department, July-Sep. 1993.
Work on automated toll collection systems

Professional In Organizing committee of CODES-ISSS 2003-2007, WASP 2003-2007, SDD 2004-2007, HLDVT 2004-2008, VTS 2008, NANOARCH 2005-2008, Program committee of SBCCI 2005-2008, CODES-ISSS 2008

PUBLICATIONS

1. I. Bayraktaroglu, J. Hunt, and D. Watkins, "Cache Resident Functional Microprocessor Testing: Avoiding High Speed IO Issues," *IEEE International Test Conference*, October 2007
2. O. Caty, P. Dahlgren, and I. Bayraktaroglu, "Microprocessor silicon debug based on failure propagation tracing," *IEEE International Test Conference*, November 2005
3. I. Bayraktaroglu, O. Caty, and Y. Wong, "Highly configurable programmable built-in self test architecture for high-speed memories," *IEEE VLSI Test Symposium,* pp. 21-26, May 2005
4. I. Bayraktaroglu and M. d'Abreu, "ATPG based functional test for data paths: application to a floating point unit," *IEEE High-Level Design Validation and Test Workshop*, pp. 37-40, November 2004
5. I. Bayraktaroglu and A. Orailoglu, "The construction of optimal deterministic partitionings in scan-based BIST fault diagnosis: mathematical foundations and cost-effective implementations," *IEEE Transactions on Computers*, vol.54(1), pp. 61-75, January 2005
6. Y. Makris, I. Bayraktaroglu, and A. Orailoglu, "Enhancing reliability of RTL controller-datapath circuits via invariant-based concurrent test," *IEEE Transactions on Reliability*, vol.53(2), pp. 269-278, June 2004
7. S. Ozev, I. Bayraktaroglu, and A. Orailolu, "Seamless test of digital components in mixed-signal paths," *IEEE Design & Test of Computers*, vol.21(1), pp. 44-55, January/February 2004
8. I. Bayraktaroglu and A. Orailolu, "Concurrent application of compaction and compression for test time and data volume reduction in scan designs", *IEEE Transactions on Computers*, vol.52(11), pp. 1480-1489, November 2003
9. O. Caty, I. Bayraktaroglu, A. Majumdar, R. Lee, J. Bell, and L. Curhan, "Instruction based BIST for board/system level test of external memories and interconnects," *IEEE International Test Conference*, pp. 961-970, October 2003
10. W. Rao, I. Bayraktaroglu, and A. Orailoglu, "Test application time and volume compression through seed overlapping," *Design Automation Conference*, pp. 732-737, June 2003

11. I. Bayraktaroglu and A. Orailoglu, "Decompression hardware determination for test volume and time reduction through unified test pattern compaction and compression," *IEEE VLSI Test Symposium,* pp. 113-118, April 2003
12. O. Sinanoglu, I. Bayraktaroglu, and A Orailoglu, "Dynamic test data transformations for average and peak power reductions," *IEEE European Test Workshop*, pp. 113-118, May 2002
13. O. Sinanoglu, I. Bayraktaroglu, and A Orailoglu, "Test power reduction through minimization of scan chain transitions," *IEEE VLSI Test Symposium*, pp. 166-171, May 2002
14. O. Sinanoglu, I. Bayraktaroglu, and A Orailoglu, "Scan power reduction through test data transition frequency analysis," *IEEE International Test Conference*, pp. 844-850, November 2002
15. I. Bayraktaroglu and A. Orailoglu, "Gate level fault diagnosis in scan-based BIST," *IEEE Design, Automation and Test in Europe*, pp. 376-381, April 2002
16. I. Bayraktaroglu and A. Orailoglu, "Cost-effective deterministic partitioning for rapid diagnosis in scan-based BIST," *IEEE Design & Test of Computers,* vol.19(1), pp. 42-53, January/February 2002
17. I. Bayraktaroglu and A. Orailoglu, "Selecting a PRPG: Randomness, primitiveness, or sheer luck?" *IEEE Asian Test Symposium*, pp. 373-378, November 2001
18. I. Bayraktaroglu and A. Orailoglu, "Concurrent test for digital linear systems," *IEEE Transactions on Computer-Aided Design*, vol.20(9), pp. 1132-1142, September 2001
19. I. Bayraktaroglu and A. Orailoglu, "Test volume and application time reduction through scan chain concealment," *Design Automation Conference*, pp. 151-155, June 2001
20. I. Bayraktaroglu and A. Orailoglu, "Diagnosis for scan-based BIST: Reaching deep into the signatures," *IEEE Design, Automation and Test in Europe*, pp. 102-109, March 2001
21. I. Bayraktaroglu and A. Orailoglu, "Improved methods for fault diagnosis in scan-based BIST," *Latin American Test Workshop*, pp. 169-172, February 2001
22. I. Bayraktaroglu and A. Orailoglu, "Accumulation-based concurrent fault detection for linear digital state variable systems," *IEEE Asian Test Symposium*, pp. 484-488, December 2000
23. I. Bayraktaroglu and A. Orailoglu, "Deterministic partitioning techniques for fault diagnosis in scan-based BIST," *IEEE International Test Conference*, pp. 273-282, October 2000
24. I. Bayraktaroglu and A. Orailoglu, "Low cost concurrent test implementation for linear digital systems," *IEEE European Test Workshop*, pp. 140-143, May 2000
25. I. Bayraktaroglu and A. Orailoglu, "Improved fault diagnosis in scan-based BIST via superposition," *Design Automation Conference,* pp. 55-58, June 2000
26. I. Bayraktaroglu and A. Orailoglu, "Unifying methodologies for high fault coverage concurrent and off-line test of digital filters," *IEEE Int. Symposium on Circuits and Systems,* pp. 705-708, May 2000
27. I. Bayraktaroglu and A. Orailoglu, "Cost effective digital filter design for concurrent test," *International Conference on Acoustic, Speech and Signal Processing,* pp. 3323-3326, June 2000
28. Y. Makris, I. Bayraktaroglu, and A. Orailoglu, "Invariance-based on-line test for RTL controller-datapath circuits," *IEEE VLSI Test Symposium,* pp. 459-464, April 2000
29. S. Ozev, I. Bayraktaroglu, and A. Orailoglu, "Test synthesis for mixed signal SOC paths," *IEEE Design Automation and Test in Europe Conference,* pp. 128-133, March 2000
30. I. Bayraktaroglu and A. Orailoglu, "Combined on-line/off-line test solutions for digital filters," *IEEE International On-Line Testing Workshop*, pp. 34-38, July 1999
31. I. Bayraktaroglu and A. Orailoglu, "Low-cost on-line test for digital filters," *IEEE VLSI Test Symposium*, pp. 446-451, April 1999
32. I. Bayraktaroglu, S. Ogrenci, G. Dundar, S. Balkir, and E. Alpaydin, "ANNSyS: An analog neural network synthesis system," *Neural Networks*, vol.12(2), pp. 325-338, March 1999
33. I. Bayraktaroglu, K. Udawatta, and A. Orailoglu, "An examination of PRPG selection approaches for large, industrial VLSI designs," *IEEE Asian Test Symposium*, pp. 440-444, December 1998
34. I. Bayraktaroglu, S. Ogrenci, G. Dundar, S. Balkir, and E. Alpaydin, "ANNSyS: An analog neural network synthesis system," *International Conference on Neural Networks*, June 1997
35. I. Bayraktaroglu, S. Ogrenci, G. Dundar, S. Balkir, and E. Alpaydin, "On-chip training by software for analog neural networks using ANNSyS," *NASA Symposium on VLSI*, March 1997
36. I. Bayraktaroglu, S. Balkir, and G. Dundar, "ANNSiS: A circuit level simulator for analog neural networks," *Turkish Symposium on Artificial Intelligence and Neural Networks*, pp. 305-310, June 1996